REMARKS

Applicants appreciate the detailed examination evidenced by the Official Action Mailed January 8, 2007 (hereinafter "Official Action"). In response, Applicants have significantly amendment independent Claims 1 and 20 to include, for example, "asserting a signal to the general operation processor circuit to prevent the operation processor circuit from accessing the programmable memory", and "transmitting an indication to outside the electronic device that the transfer of program data to the programmable memory is complete", "and then de-asserting the signal to the general operation processor circuit to allow the general operation processor circuit to access the programmable memory," without using "random access memory and read-only memory devices" where transfer of the data is performed to a " buffer circuit coupled to the programmable memory."

Applicants have also added new dependent claims 27 and 28, which recite that the buffer circuit is particularly sized for a "word or sector" and configured to store this amount of data, which is not disclosed or suggested by any of the cited references.

Applicants respectfully submit that none of the cited references, taken either singularly or in combination, discloses or suggests the detailed recitations of the amended claims. Accordingly, Applicants respectfully request the withdrawal of all rejections, the allowance of all claims for at least the reasons described herein.

The objections to the drawings have been overcome by amendment.

The drawings stand rejected to over 37 CFR § 1.121 (d). Official Action, page 3. In response, Applicants provide herewith both an annotated original drawing as well as a formalized replacement sheet (labeled appropriately), wherein the original Korean language text has been replaced with the English language equivalents "Stop" and "Start" as shown. Applicants respectfully request the Examiner's approval of the proposed drawing changes and withdrawal of the objection of the drawings.

The objections to the claims have been overcome by amendment.

Claim 25 stands objected to over the recitation of "recycling" in line 2. Official Action, page 3. In response, Applicants have amended Claim 25 to recite "cycling power provided to the controller circuit..." as suggested by the Examiner. Accordingly, Applicants respectfully request withdrawal of the objection to Claim 25.

The Amended Claims Comply with § 112

Claims 1-10, 21-22 and 24-25 stand rejected under 35 U.S.C. § 112, second paragraph. The Official Action, page 3. In particular, Claim 1 stands rejected over recitations that the programmable memory and the controller circuit are "separate from a general operation processor circuit." In response, Applicants submit that the recitation of separate (as described in this specification) provides an adequate description of the nature of the programmable memory and the controller circuit (relative to the general operation processor circuit) as required under §112, second paragraph. For example, as described in the specification at page 8, lines 19-26:

> The controller circuit 125 can transfer the program from the programming system 105 over the interface to the programmable memory, while the general operation processor circuit 110 is unable to access the programmable memory 120 while the controller circuit 125 is transferring the program data.

Accordingly, Applicants respectfully submit that the recitation of separate as appearing these claims complies with §112, second paragraph. Alternatively, if the Examiner still believes that such recitations do not comply with those requirements, Applicants submit that these recitations could be removed from independent Claims 1 and 20 by further amendment.

Claims 2-10 and 24-25 as well as claims 21-22 stand rejected over recitation of "A" in the first line of each of these dependent claims. Although Applicants maintain that the recitation of "A" in the context of a dependent claim does not render such claims indefinite, Applicants have amended each of the dependent claims to recite "The" as suggested by the Examiner. Applicants note, further, that these claims have not been amended for reasons related to patentability and, therefore, a full range of equivalents remains available for these claims. Accordingly, the rejections of these

claims have been overcome and are respectfully requested to be withdrawn.

Amended independent Claims 1 and 20 are patentable over the cited references.

Claims 1-3, 6-10, and 20-21 stand rejected under 35 U.S.C. § 102 over U.S. Patent No. 5,968,141 to Tsai (Tsai '141). *Official Action, page 5.* In response, Applicants have amended the independent Claims significantly to further clarify the present subject matter relative to the cited references. For example, independent Claim 1 has been amended to recite in part:

> transferring program data from outside the electronic device to **a buffer circuit** coupled to a programmable memory in the electronic device via a controller circuit, **without using Random Access Memory (RAM) and Read Only Memory (ROM) devices that are separate from the controller circuit**, that controls programming of the programmable memory in the electronic device that is separate from a general operation processor circuit used to provide general operations of the electronic device subsequent to transferring the program data into the programmable memory;
>
> **asserting a signal to the general operation processor circuit to prevent the general operation processor circuit from accessing the programmable memory during transfer of program data into the programmable memory;**
>
> **transmitting an indication to outside the electronic device that the transfer of program data to the programmable memory is complete; and then**
>
> **de-asserting the signal to the general operation processor circuit to allow the general operation processor circuit to access the programmable memory.**

Independent Claim 20 has been similarly amended.

Applicants respectfully submit that Tsai '141, for example, does not disclose or suggest "transferring program data from outside the electronic device to a buffer circuit coupled to a programmable memory..." To the contrary, Figure 3 of Tsai '141 shows that program data is transferred through the program controller 32 to the multiplexer 36 for presentation to the non-volatile memory 34. Accordingly, Figure 3 of Tsai '141 shows that there is no transfer to a buffer circuit coupled to the programmable memory of the electronic device as claimed.

Applicants also submit that Tsai '141 does not disclose or suggest "asserting a signal to the general operation processor circuit to prevent the general operation

processor circuit from accessing the programmable memory during transfer of program data into the programmable memory," as illustrated, for example, in Figure 2 of Applicant's disclosure. To the contrary, Tsai '141 describes the operation of the microcontroller 33 relative to the non-volatile memory 34 as follows:

> Thus, as is illustrated in FIG. 3, the apparatus of the invention for upgrading the firmware cod of optical disk drive via the ATA/IDE interface has a multiplexer (MUX) 36 arranged between the microcontroller 33 and the firmware code memory 34 of the drive control electronic circuitry 30. In addition to the decode processing performed by the CD-ROM decoder 31, **a programming controller (PRG CNTL) 32 is used to steer the multiplexer 36 for selectively connecting the memory device 34 either to the microcontroller 33 for normal mode of operation or to the IDE bus 10 for connection with the host processor in the firmware** upgrade mode of operation. In order to achieve this, as is shown in FIG. 3, the multiplexer 36 is basically a two-to-one multiplexing device, whose details will be covered below. (Tsai '141, column 6, lines 19-33. Emphasis added.)

As indicated by the above-cited passage from Tsai '141, the program controller 32 disables the path between the multiplexer 36 and the non-volatile memory 34 so that the microcontroller 33 is unable to access the non-volatile memory 34. However, there is no disclosure or suggestion that a signal is asserted to the microcontroller 33 to prevent access to the programmable memory during transfer of program data to the programmable memory as claimed. Accordingly, Tsai '141 also does not disclose or suggest these recitations of independent Claims 1 and 20.

Tsai '141 also does not disclose or suggest "de-asserting the signal to the operation processor circuit to allow the general operation processor circuit to access the programmable memory." To the contrary, as discussed above, Tsai '141 does not disclose or suggest any transmission of a signal to the microcontroller 33 controlling the microcontroller's access to the non-volatile memory 34. Actually, the program controller 32 controls the multiplexer 36 to prevent access to the non-volatile memory 34 by the microcontroller 33. Accordingly, Tsai '141 does not disclose or suggest these recitations of the amended independent claims.

Furthermore, Tsai '141 does not disclose or suggest "transmitting an indication to outside the electronic device that the transfer of program data to the programmable memory is complete." To the contrary, Tsai '141 reads as follows:

> The other route that can be established to the firmware code storage memory device is for the memory device itself to be directly accessible by the host computer system when a code upgrade is ordered. In this mode of operation, the multiplexer connects the memory device to the IDE interface of the optical disk drive unit, so that the processor of the host system can directly access the memory space of the firmware memory. This direct access includes both writing into and reading from the memory device. **The ability to read from the memory device is necessary at it is a means to verify whether or not the correct content of programming has been achieved**. (Tsai '141, column 6, lines 1-12. Emphasis added).

Although the above passage of Tsai '141 does discuss verifying whether or not the correct content was programmed to the non-volatile memory 34, there is no disclosure or suggestion that such an indication is transmitted to outside the electronic device. Accordingly, Applicants respectfully submit that Tsai '141 also does not disclose or suggest these recitations of amended independent Claims 1 and 20.

In addition to the above, Applicants further submit that the remaining cited references: U.S. Patent No. 6,295,053 to Tsai, et al. ("Tsai '053") and U.S. Patent No. 6,507,881 to Chen ("Chen"), do not disclose or suggest the combinations of recitations show above to be missing from Tsai '141. For example, Chen describes the transfer of programmable data as follows:

> "If several flash ROM programming cycles are needed in one host request, the firmware can be temporarily stored into a buffer, **such as a RAM and then sequentially written into the flash ROM through the flash controller**. Since the software method may occupy too much time of the IDE interface, resulting in a delay for the other subsequent activities, the hardware method may be a better way to update the firmware code, particularly to a large firmware code. (Abstract of Chen, Emphasis added)

As indicated by the above-cited passage of Chen, the approach therein employs a Random Access Memory to store data transferred from a host to the NVM. In contrast, amended independent Claims 1 and 20 recite that data is transferred from outside the electronic device to a "buffer circuit" but "without using Random Access Memory (RAM) and Read Only Memory (ROM) devices." As shown above, Chen employs a RAM to store data temporarily before programming to the non-volatile memory. Accordingly, Chen also does not disclose or suggest at least these recitations of the amended independent claims.

Furthermore, there is no disclosure or suggestion in either Chen or Tsai '053 of transmitting a signal to a processor (dedicated to the operation of the electronic device being programmed) to prevent the processor from accessing the programmable memory during the transfer of program data to the programmable memory as recited in the amended independent claims.

There is further no disclosure or suggestion in Chen and/or Tsai '053 of de-asserting a signal to the processor circuit to allow the processor circuit to access the programmable memory (once the data transfer is complete) as recited in the amended independent claims.

In view of the above, even if the cited references were combined, the combination would not disclose or suggest many of the recitations of the amended independent claims as required under § 103.

Furthermore, there is no clear and particular evidence of a motivation or suggestion to combine these references as required under § 103. For example, Tsai '141 calls for a parallel interface used as part of an IDE bus interconnect for a CD-ROM. In contrast, Tsai '053 calls for a serial interface (see for example Figures 5, 8, and 9), which is incompatible with the implementation shown in Tsai '141 (*i.e.*, a parallel IDE interface). In particular, as shown in Figure 4 of Tsai '141, control of the multiplexer 32 relies upon the static nature of control signals to maintain the setting of the multiplexer circuit so that the program controller 32 can maintain control over the non-volatile memory 34 to complete the transfer. However, if (as would be the case in a serial transfer) the control signals used to control the state of the multiplexer 36 were to be transitional (*i.e.* transition on/off during a serial transfer as opposed to a parallel transfer over the IDE bus) the microcontroller 33 may be provided an opportunity to access the non-volatile memory 34 (during times when the programmable memory could be accessed by the microcontroller because of the transitional nature of the control signals during the serial transfer). Accordingly, Applicants respectfully submit that there is no clear and particular evidence of a motivation or suggest to combine Tsai '141 with Tsai '053 as to do so could render either one of these two references inoperable for their intended purpose.

Applicants also respectfully submit that there is no clear and particular

evidence of a motivation or suggestion to combine Tsai '141 with Chen. In particular, both Tsai '141 and Chen call for an IDE interface to a CD-ROM to be used to program a non-volatile memory controlling the operation of the CD-ROM. Accordingly, Applicants respectfully submit there is no clear and particular evidence of a motivation or suggestion to combine these references as both references achieve the same objective. Accordingly, Applicants respectfully submit that there is no clear and particular evidence of motivation or suggestion to combine the cited references as required under § 103.

In view of the above, Applicants respectfully submit that amended independent Claims 1 and 20 are patentable over the cited references for at least the reasons described above. Furthermore, dependent Claims 3-5, 7, 10 and 24-25 are patentable over the cited references for at least the reasons described above in reference to the amended independent Claims.

CONCLUSION

Applicants have significantly amended independent Claims 1 and 20 as described above. Furthermore Applicants have provided remarks as to why there is no disclosure or suggestion of many of the recitations of the amended independent Claims and further, there is no clear and particular evidence of a motivation or suggestion to combine the cited references as required under § 103. Accordingly, Applicants respectfully request the withdrawal of all rejections, and the allowance of all claims in due course. If any informal matter should arise the Examiner is encouraged the undersigned by telephone.

Respectfully submitted,

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